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EXAMINER

FOWLKES, ANDRE R

ART UNIT

PAPER NUMBER

2192

DATE MAILED: 04/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-------------------------------|------------------------------------|--|
| Office Action Summary | Application No. 09/924,260 | Applicant(s) DUESTERWALD ET AL. | |
| | Examiner Andre R. Fowlkes | Art Unit 2192 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 November 2004.
2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20,22 and 23 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-20,22 and 23 is/are rejected.
7) ☐ Claim(s) 22 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. This action is in response to the amendment filed 11/4/04.

Claim Objections

2. The objection to claims 7 and 9 are withdrawn, in view of applicant's amendment.
3. Claim 22 is objected as it is dependant on a rejected base claim. The examiner is interpreting claim 22 as depending from claim 20.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-8, 11, 16, 17 and 20, 22 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Bugnion, U.S. Patent No. 6,704,925.

As per claim 1, Bugnion discloses an **apparatus for dynamically transforming and caching at least one computer program**, (col. 1:61-65, "Dynamic binary translators perform the translation from an original instruction sequence to a host instruction sequence during the execution of the program. The translated code sequences are then stored in a buffer called the translation cache"), **the apparatus comprising:**

- **one or more computer readable storage media** (col. 4:27-28, "The output instruction sequences are stored in a translation cache (computer readable storage media)"),

- **computer executable instructions stored in the one or more computer readable storage media**, (col. 4:27-28, "The output instruction sequences are stored in a translation cache"), **the computer executable instructions comprising:**

- **instructions for dynamically transforming code fragments** (col. 1:61-65, "Dynamic binary translators perform the translation from an original instruction sequence to a host instruction sequence during the execution of the program. The translated code sequences are then stored in a buffer called the translation cache"),

- **instructions for caching said code fragments** (col. 4:27-28, "The output instruction sequences are stored in a translation cache"),

- **instructions for causing said code fragments to be executed by at least one computer processor** (col. 5:29-30, "the system then executes the output instruction"),

- **instructions providing an application programming interface enabling said at least one computer program to activate said instructions for dynamically transforming said code fragments and said instructions for caching said code fragments** (col. 6:3, Bugnion discloses the applications necessary to communicate with the "operating system" or some other system or control program programs (i.e. application programming interfaces)).

As per claim 2, the rejection of claim 1 is incorporated and further, Bugnion discloses that **said instructions providing an application programming interface enable said at least one computer program to provide said code fragments for said instructions for dynamically transforming code fragments and for said instructions for caching said code fragments** (col. 6:3, Bugnion discloses applications to communicate with the "operating system" or some other system or control program programs (i.e. application programming interfaces), and col. 1:61-65, "Dynamic binary translators perform the translation from an original instruction sequence to a host instruction sequence during the execution of the program. The translated code sequences are then stored in a buffer called the translation cache").

As per claim 3, the rejection of claim 1 is incorporated and further, Bugnion discloses that **said instructions providing an application programming interface include providing functions for caching and executing a specified code fragment** (col. 6:3, Bugnion discloses applications to communicate with the “operating system” or some other system or control program programs (i.e. application programming interfaces), and col. 1:61-65, “Dynamic binary translators perform the translation from an original instruction sequence to a host instruction sequence during the execution of the program. The translated code sequences are then stored in a buffer called the translation cache”).

As per claim 4, the rejection of claim 1 is incorporated and further, Bugnion discloses that **said instructions providing an application programming interface include providing functions for configuring behavior of said instructions for dynamically transforming said code fragments and said instructions for caching said code fragments** (col. 6:3, Bugnion discloses an application to communicate with the “operating system” or some other system or control program programs (i.e. application programming interfaces), and functions for configuring the translation system)

As per claim 5, the rejection of claim 1 is incorporated and further, Bugnion discloses that **said instructions for dynamically transforming said code fragments comprise instructions for changing memory address references in said code**

fragments (col. 3:38-40, "translate each data reference from a virtual address issued by the simulated processor to a physical address").

As per claim 6, the rejection of claim 1 is incorporated and further, Bugnion discloses that **said instructions for dynamically transforming said code fragments comprise instructions for changing the layout of said code fragments while preserving the function of said code fragments** (col. 8:1, "compiler optimizations (e.g. code motion, which changes the layout of code, while preserving the original function").

As per claim 7, the rejection of claim 1 is incorporated and further, Bugnion discloses that **said instructions providing an application programming interface include instructions for accessing code fragments a cross a network** (col. 6:3, "computer system (i.e. networked computers", and col. 6:3, Bugnion discloses an application to communicate with the "operating system" or some other system or control program programs (i.e. application programming interfaces)).

As per claim 8, the rejection of claim 1 is incorporated and further, Bugnion discloses that **at least one computer program comprises at least one emulator** (col. 4:25-26, "(a computer programs that) emulate the corresponding input instruction sequences").

As per claim 11, the rejection of claim 1 is incorporated and further, Bugnion discloses that **at least one computer program comprises at least one operating system** (col. 6:3, "operating system").

As per claim 16, the rejection of claim 1 is incorporated and further, Bugnion discloses that **said computer executable instructions further comprising instructions for optimizing said code fragments** (col. 8:1, "(code) optimizations").

As per claim 17, the rejection of claim 1 is incorporated and further, Bugnion discloses that **said computer executable instructions further comprising instructions for linking a plurality of said code fragments to create a larger code fragment** (col. 8:1, "(code) optimizations (e.g. replacing a function call, with the actual code for the function, creating a larger, more efficient code fragment)").

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. Claims 9, 10, 12-15, 18, 19, 20, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugnion, U.S. Patent No. 6,704,925 in view of Yates et al., (Yates), U.S. Patent No. 5,802,373.

As per claim 9, the rejection of claim 1 is incorporated and further, Bugnion doesn't explicitly disclose that **at least one computer program comprises a plurality of emulators being executed simultaneously**.

However, Yates, in an analogous environment, discloses that **at least one computer program comprises a plurality of emulators being executed simultaneously** (col. 15:45-48, "emulate multiple addressing spaces which are possible in the Intel architecture and other non-native architectures").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Yates into the system of Bugnion to have **at least one computer program comprises a plurality of emulators being executed simultaneously**. The modification would have been obvious because one of ordinary skill in the art would have wanted the option of executing multiple emulators for different computer architectures at the same time.

As per claim 10, the rejection of claim 9 is incorporated and further, Bugnion discloses that **said plurality of emulators comprise emulators for at least two different computer architectures** (col. 4:25-26, "(a computer programs that) emulate

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the corresponding input instruction sequences”, and the phrase “Depending on the system architecture”, at col. 10:14 , indicates several different computer architectures).

As per claim 12, the rejection of claim 1 is incorporated and further, Bugnion doesn't explicitly disclose that said computer executable instructions further comprising instructions for **transparently obtaining said code fragments from said at least one computer program** for said instructions for dynamically transforming said code fragments and for said instructions for caching said code fragments.

However, Yates, in an analogous environment, discloses that said computer executable instructions further comprising instructions for **transparently obtaining said code fragments from said at least one computer program** for said instructions for dynamically transforming said code fragments and for said instructions for caching said code fragments (col. 15:11-12, “to transparently emulate the execution of a ... non-native instruction”).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Yates into the system of Bugnion to have a instructions for **transparently obtaining said code fragments from said at least one computer program**. The modification would have been obvious because one of ordinary skill in the art would be motivated to allow existing software to be translated and executed on new hardware while excluding the details from the software user in order to minimize distractions and unnecessary details for a new or novice computer user.

As per claim 13, the rejection of claim 12 is incorporated and further, Bugnion discloses that **said computer executable instructions further comprising instructions for controlling the execution of said at least one computer program on said at least one computer processor** (col. 1:61-65, "Dynamic binary translators perform the translation from an original instruction sequence (i.e. instructions for controlling the execution of a program on a processor) to a host instruction sequence during the execution of the program").

As per claim 14, the rejection of claim 12 is incorporated and further, Bugnion discloses that **said computer executable instructions further comprising instructions for obtaining optimal portions of code from said at least one computer program to create said code fragments** (col. 1:61-65, "Dynamic binary translators perform the translation from an original instruction sequence (i.e. instructions for controlling the execution of a program on a processor) to a host instruction sequence during the execution of the program", and col. 8:1, "(code) optimizations").

As per claim 15, the rejection of claim 1 is incorporated and further, Bugnion discloses that **said instructions for transparently obtaining said code fragments from said at least one computer program obtain said code fragments across a network** (col. 6:3, "computer system (i.e. networked computers", and col. 6:3, Bugnion

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discloses an application to communicate with the "operating system" or some other system or control program programs (i.e. application programming interfaces)).

As per claim 18, the rejection of claim 1 is incorporated and further, Bugnion doesn't explicitly disclose that **said computer executable instructions further comprising instructions for replacing hardware control code in said code fragments, where said hardware control code is adapted to control hardware which is not present and hardware which is not functioning**

However, Yates, in an analogous environment, discloses that **said computer executable instructions further comprising instructions for replacing hardware control code in said code fragments, where said hardware control code is adapted to control hardware which is not present and hardware which is not functioning** (col. 1:15-18, "(the system) includes all of the software resources needed by the computer system to interface each of the hardware elements to the computer system", and these instructions are then translated (i.e. replaced)).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Yates into the system of Bugnion to have **said computer executable instructions further comprising instructions for replacing hardware control code in said code fragments, where said hardware control code is adapted to control hardware which not present and hardware which is not functioning**. The modification would have been obvious because one of ordinary skill in the art would be motivated to allow the software to

exhibit all of the new hardware functionality when it is translated to a different architecture system.

As per claim 19, this is another apparatus version of the claimed apparatus discussed above, in claims 12, 16 and 18 wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Bugnion fig. 2, translation system and Yates col. 15:11-12 and col. 1:15-18.

As per claims 20 and 22, this is another apparatus version of the claimed apparatus discussed below, in claim 23, wherein all claimed limitations have also been addressed and/or cited as set forth below. For example, see Bugnion fig. 2, translation system and associated text.

As per claim 23, the rejection of claim 9 is incorporated and further, Bugnion doesn't explicitly disclose that **said plurality of emulators are executed simultaneously on said at least one computer processor using a single instantiation of said instructions for dynamically transforming code fragments.**

However, Yates, in an analogous environment, discloses that **said plurality of emulators are executed simultaneously on said at least one computer processor using a single instantiation of said instructions for dynamically transforming code fragments** (col. 15:45-48, "emulate multiple addressing spaces (using a single

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instantiation) which are possible in the Intel architecture and other non-native architectures”).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Yates into the system of Bugnion to have **said plurality of emulators are executed simultaneously on said at least one computer processor using a single instantiation of said instructions fro dynamically transforming code fragments**. The modification would have been obvious because one of ordinary skill in the art would have wanted the convenience of controlling multiple emulators with a single instantiation.

Response to Arguments

Applicants arguments have been considered but they are not persuasive.

In the remarks, the applicant has argued substantially that:

1) Bugnion does not disclose instructions providing an application programming interface enabling said at least one computer program to activate said instructions for dynamically transforming said code fragments and said instructions for caching said code fragments, at p.9:15-11:7 and 14:25-15:24.

Examiner's response:

1) The examiner disagrees with applicant's characterization of the applied art. An API is the set of routines, data structures, constants, and other programming elements

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that allow developers to use some part of the system software. Bugnion discloses the set of routines, data structures, constants, and other programming elements that allow developers to use the system for dynamically transforming said code fragments and said instructions for caching said code fragments.

In the remarks, the applicant has argued substantially that:

2) The cited references do not disclose a plurality of emulators being executed simultaneously, at p. 11:17-12:12 and 15:25-16:20.

Examiner's response:

2) See the art rejection to amended claim 9, above.

In the remarks, the applicant has argued substantially that:

3) Bugnion does not disclose that said plurality of emulators comprise emulators for at least two different computer instruction set architectures, at p. 12:13-24 and p. 16:21-17:3.

Examiner's response:

3) See the art rejection to amended claim 9, above.

In the remarks, the applicant has argued substantially that:

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- 4) The cited references do not disclose instructions for replacing hardware control code that is adapted to control non-functioning hardware, at p. 13:3-14:7.

Examiner's response:

- 4) Yates discloses at col. 1:15-18, that "(the system) includes all of the software resources needed by the computer system to interface each of the hardware elements to the computer system (functional and non-functional)", and these instructions are then translated (i.e. replaced))

In the remarks, the applicant has argued substantially that:

- 5) The cited references do not disclose the limitations of new claim 23.

Examiner's response:

- 5) See art rejection to new claim 23, above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

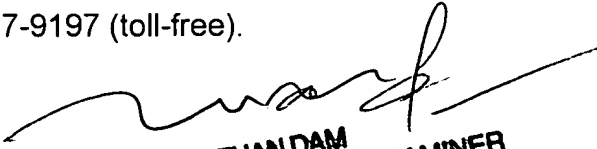
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: 571-272-2100.**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre R. Fowlkes whose telephone number is (571) 272-3697. The examiner can normally be reached on Monday - Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


TUAN DAM
SUPERVISORY PATENT EXAMINER

ARF